NIR Sensitivity Enhanced 55nm BCDLite® FSI SPAD

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The rising demand for exceptional performance is fueling advancements in high-sensitivity devices that can operate in the near-infrared (NIR) spectrum, delivering unmatched results across diverse applications, from enabling the autonomous navigation of vehicles through advanced LiDAR systems to facilitating non-invasive medical diagnostics via optical coherence tomography. Within this landscape of increasing demand, solid-state photodetectors such as single-photon avalanche diodes (SPADs) thrive due to their photon counting capability, low jitter, and noise levels. These features make them an invaluable asset in various applications. The recent industrialization of SPADs, enabling their fabrication within standard CMOS technology nodes, has significantly reduced production costs and increased design flexibility [1-4], facilitating wider adoption. Although these devices are now available in some standard technologies, substantial and multidisciplinary effort is spent in their design and continuous improvement to meet the evolving and increasingly stringent performance demands of customers. A key point is the optimization of the junction profiles to guarantee the proper breakdown voltage and an effective charge collection without compromising the device noise. In the presented work, we revised the design presented in [1] to obtain a notable improvement in NIR photon detection probability (PDP) and dark count rate (DCR) and studied the performance dependency over a range of device's active area. Figure 1 depicts the schematic device cross-section and the corresponding TCAD 2D electric field simulation. The simulation results reveal a uniform high-field region localized at the device junction, with no evidence of edge breakdown. This finding is corroborated by the light emission test, which shows uniform light emission across the SPAD's active area, as illustrated in Figure 2 (*bottom-left*). Figure 2 presents the characterization results for three device sizes (i.e., 10 µm, 12 µm, and 16 µm), showcasing the breakdown voltage versus temperature, the DCR trend, and the Arrhenius plot over a broad temperature range. At room temperature, the devices have a breakdown voltage of approximately 21.4 V, with a temperature coefficient of about 18.8 mV/K. To ensure compatibility with standard logic devices and minimize power consumption, the presented SPADs are optimized for operation around 2 V excess bias (Vex). Under these conditions, the DCR is lower than that reported in [1], with a median value of about 9.2 cps, 23.6 cps, and 81.8 cps for a 10 µm, 12 µm, and 16 µm size, respectively, at 2 V excess bias (Vex) and room temperature. These values translate to a normalized DCR of about 0.22 cps/µm^2, 0.33 cps/µm^2, and 0.53 cps/µm^2, respectively.

A detailed analysis of the DCR as a function of temperature, as depicted in the Arrhenius plot in Figure 2 (right), revealed a strong temperature dependence above 0°C for all the tested devices. This observation confirms that thermal generation, rather than band-to-band tunneling, is the dominant mechanism contributing to the DCR at room temperature. The normalization of DCR by the active area (cps/µm²) allows for a direct comparison of device performance across different sizes. This metric is particularly important for evaluating the scalability of the

SPAD technology and understanding the impact of edge effects on DCR. The low normalized DCR achieved in our devices demonstrates the effectiveness of our optimized process and junction profiles in minimizing dark counts across different active areas, highlighting the robustness of the design, as shown in Fig 3 (*left*). The engineered doping profiles of the presented SPAD lead to an exceptional median PDP value of approximately 4.5% at 940 nm with 2 V Vex for device 12 µm and larger size. Figure 3 (*right*) illustrates how the optimized profiles mitigate edge effects at the device junction, which primarily contribute to the problem of lower PDP at smaller device sizes. Figure 4 presents the PDP characteristics of the fabricated SPADs, providing valuable insights into their spectral response and performance under varying operating conditions. The left plot in Figure 4 illustrates the PDP spectrum as a function of wavelength for three different SPAD sizes (10 µm, 12 µm, and 16 µm), all fabricated with the optimized doping profiles. This data reveals the spectral sensitivity of the SPADs in the near-infrared region, showing the PDP variation across a wavelength range from 780 nm to 1000 nm. Notably, the plot highlights how the PDP performance above 900 nm of the devices of 12 µm and 16 µm match quite well. The right plot in Figure 4 compares the PDP of the 12 µm SPAD device at three different excess bias voltages (1 V, 2 V, and 3 V), contrasting the performance of the process of record (POR) doping profiles (dashed lines with full circles) with the optimized doping profiles (solid lines with open diamonds). This comparison demonstrates the impact of excess bias on the PDP and highlights the improvement in PDP achieved with the optimized doping profiles.

The timing performance of the 12 µm SPAD device was evaluated using a 940 nm picosecond pulsed laser diode. Figure 5 presents the instrument response function (IRF) measured using time-correlated single photon counting (TCSPC) for both the POR (left) and optimized (right) devices at four different excess bias voltages (1 V, 2 V, 3 V, and 4 V). The timing jitter, extracted from the full width at half maximum (FWHM) of the IRF, was approximately 150 ps for the POR device and approximately 135 ps for the optimized device at 2 V excess bias (Vex). These jitter values include the contribution from the laser pulse width, which is approximately 50 ps. All measurements presented in this work were conducted at the wafer level using an external quenching resistor. While this configuration is suitable for characterizing many device parameters, it is not optimal for assessing timing jitter due to the added parasitic effects introduced by the external resistor. A significant improvement in jitter performance is expected when the SPADs are integrated into pixels with on-chip quenching circuits. Despite the limitations of the current measurement setup, the achieved PDP results are, to the best of our knowledge, among the highest reported in the literature for FSI-isolated SPAD devices.

	Units	This work			ISSW24 [1]	[3]	[2]	[4]
Size	µm	**10**	**12**	**16**	12	20.5	na	na
Technology node	nm	**55**	**55**	**55**	55	130	40	55
Fill Factor	%	**~41**	**~50**	**~60**	~50	~15.2	70	25
Median VBD (293K)	V	**21.4**	**21.4**	**21.4**	18	13.82	15.5	17.7
Median VBD Temp. Coeff.	mV/K	**18.6**	**18.6**	**18.6**	15.4	9.4	na	16
Median DCR (293K, 1V)	cps	**na**	**na**	**na**	9	~80	50	na
Median DCR (293K, 2V)	cps	**9.2**	**23.6**	**81.8**	30	~400	na	na
Median DCR (293K, 3V)	cps	**na**	**na**	**na**	56	~1000	na	0.28/µm^2
Median PDP (293K, 1V)	%	**na**	**na**	**na**	2	1.4	1.7[b]/2.2[a]	na
Median PDP (293K, 2V)	%	**3.5**	**4.35**	**4.5**	3.3	na	na	1.3
Median PDP (293K, 3V)	%	**na**	**na**	**na**	3.7	na	na	1.5
Median Timing Jitter	ps	**na**	**135**	**na**	150	>140[c]	170	>126[d]
Integrated pixel	-	**no**	**no**	**no**	no	yes	yes	no
Microlenses	-	**no**	**no**	**no**	no	no	yes	no

[a]with microlense;[b]without microlenses;[c]reported at 1.2 V;[d]reported at 1.5V

Table 1: SPAD performance comparison.

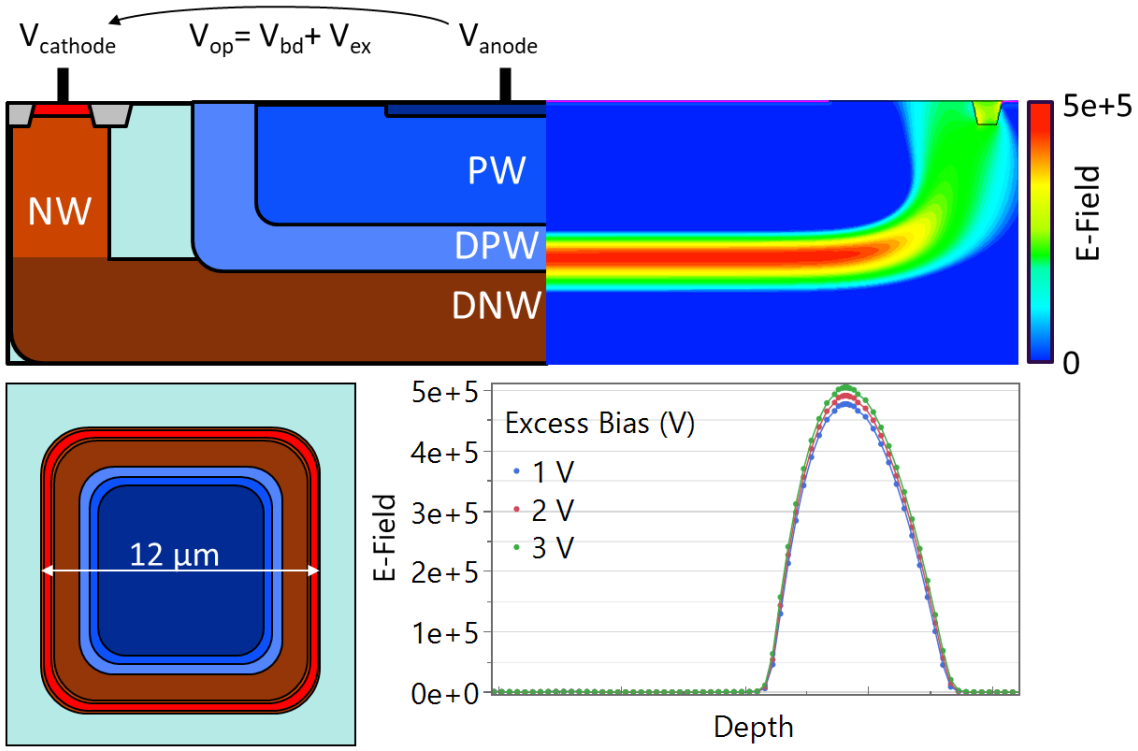

Figure 1: Cross-section of the proposed device (*top-left*) and 2D Electric Field TCAD simulation (*top-right*); Top view of the SPAD with square shape and round corner (*bottom-left*); electric-field profile across depth in the center of the device (*bottom-right*).

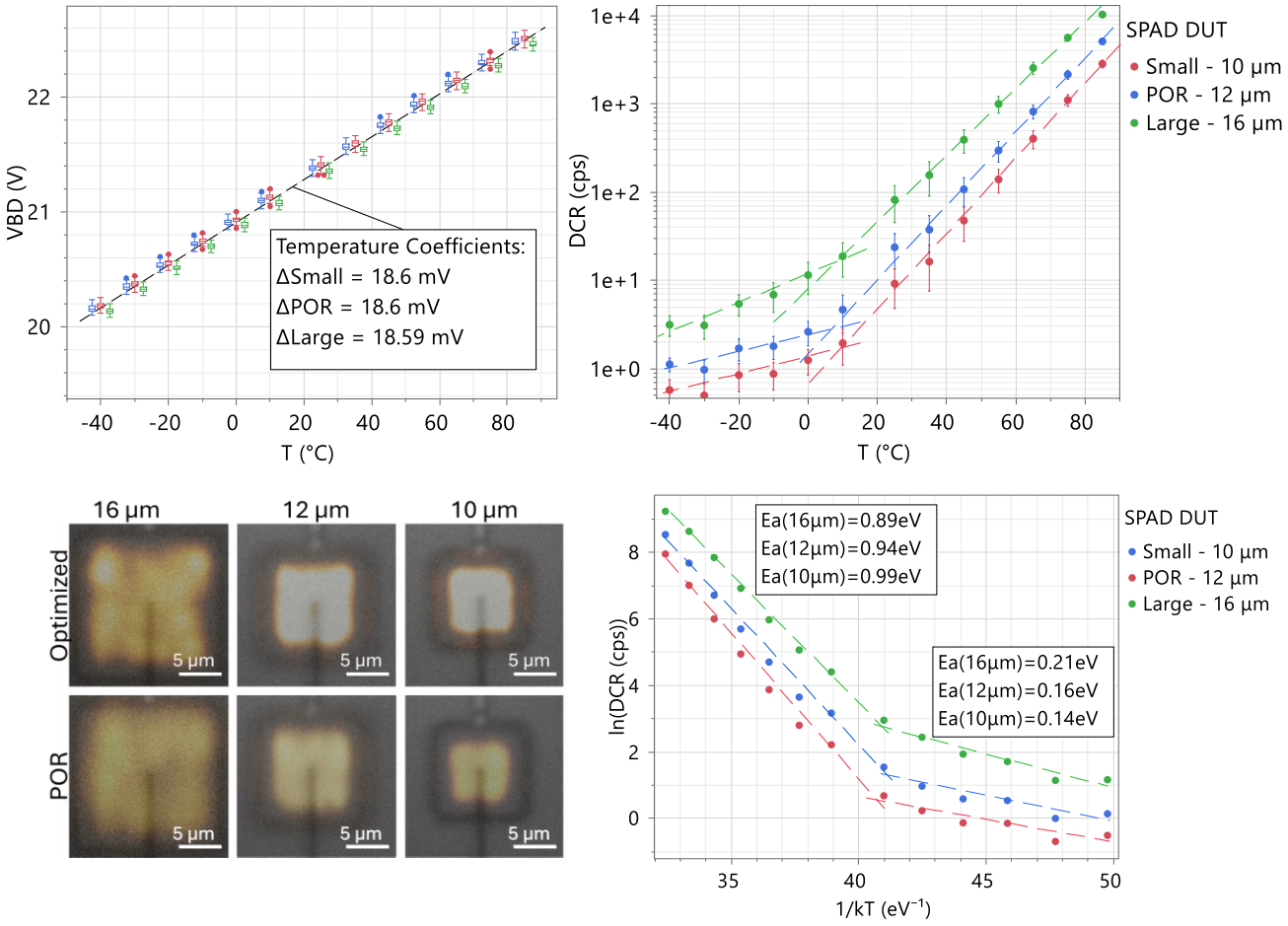

Figure 2: Breakdown (*top-left*) and DCR (*top-right*) over temperature measurement results. Light emission test (*bottom-left*) and Arrhenius plot of DCR with extracted activation energies (*bottom-right*).

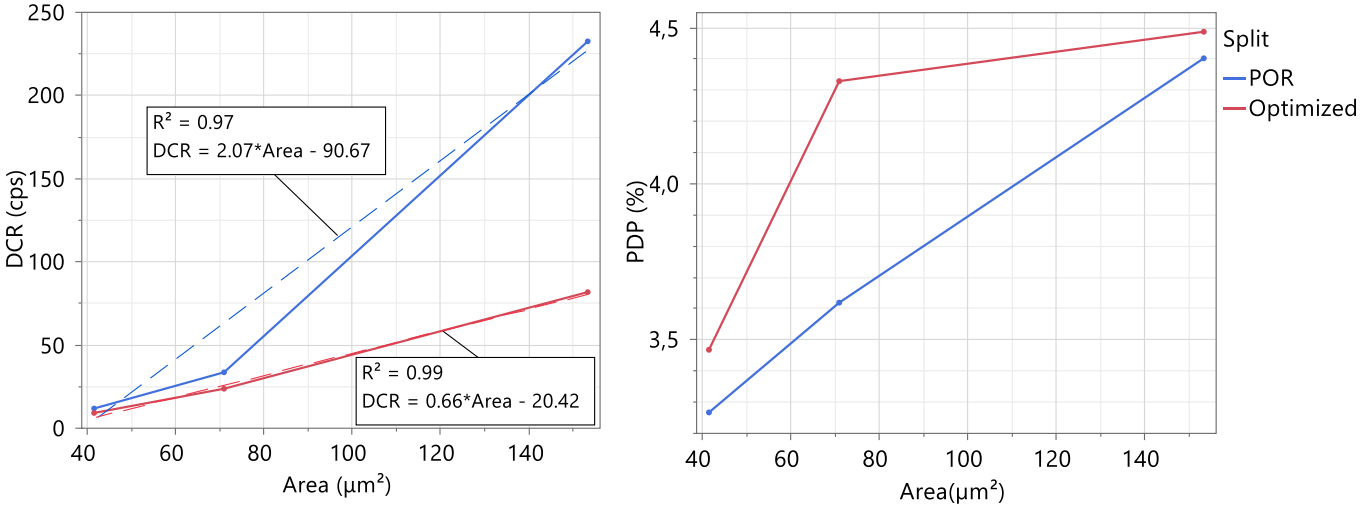

Figure 3: Median DCR (*left*) and median PDP (*right*) measured for devices with different device active area.

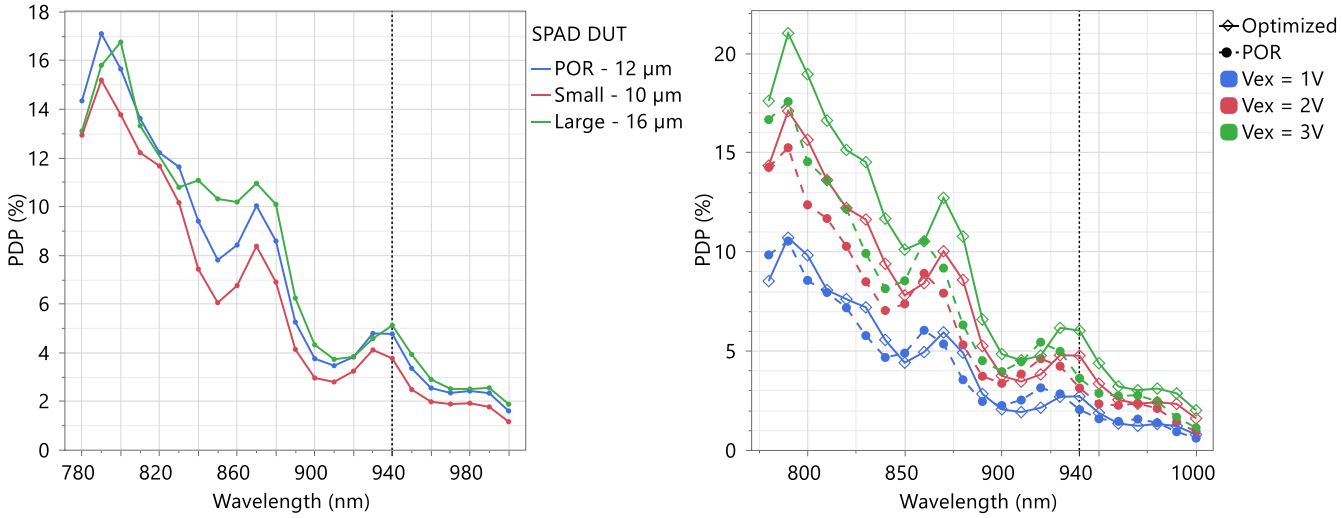

Figure 4: PDP spectrum over wavelength for the three SPAD sizes with optimize profiles (*left*) and PDP comparison for the 12 µm SPAD at three excess bias voltages (*right*) for POR (*dashed line with full circle*) and optimized (*solid line with open diamond*) doping profiles.

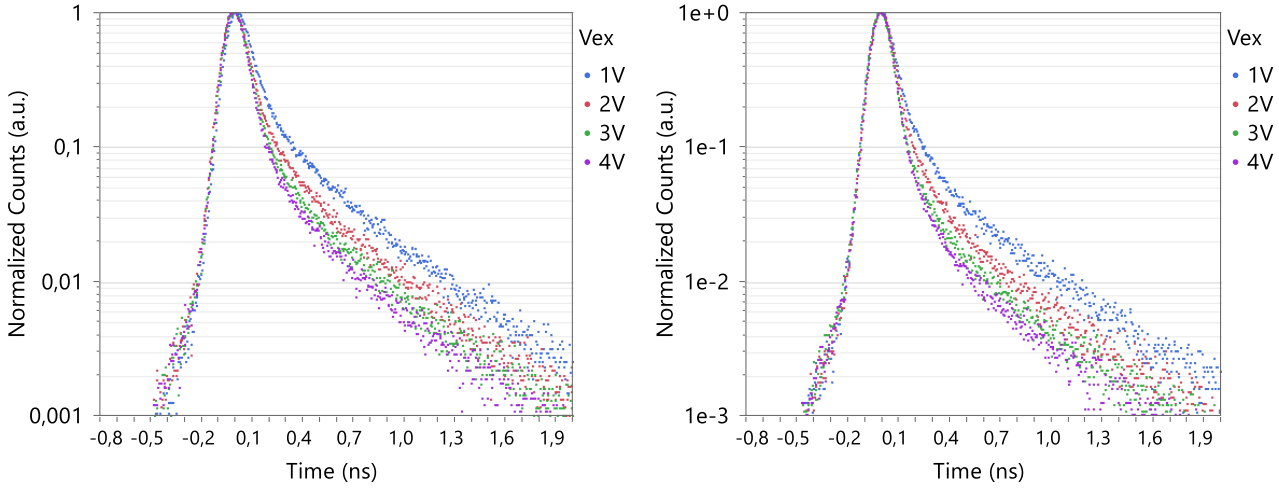

Figure 5: TCSPC IRF at 940 nm for the 12 µm size POR (*left*) and optimized (*right*) devices.

References: 1. *F. Gramuglia, et al., "*A 55nm BCDLite® FSI SPAD with Improved NIR Sensitivity and DCR*", in ISSW 2024.* **2.** S. Pellegrini, *et al.*, "Industrialised SPAD in 40 nm technology," in IEEE International Electron Devices Meeting (IEDM), 12 2017, pp. 16.5.1–16.5.4. **3.** S. Pellegrini and B. Rae, "Fully industrialised single photon avalanche diodes." Advanced Photon Counting Techniques XI. Vol. 10212. SPIE, 2017. **4.** R. Kappel, "Multizone, multiobject d-tof system in 55nm," in International SPAD Sensor Workshop (ISSW), 2018.